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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,044	08/25/2000	CHANDRA V. MOULI	MIO 0054 PA	6800

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,044	MOULI ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 45-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-12,14,45,47 and 49-57* is/are rejected.

7)☒ Claim(s) *2,4,13,46 and 48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 45 is rejected under 35 U.S.C. 102(e) as anticipated by Kusunoki et al. (6,335,549).

Kusunoki et al. teach in figure 1 and related text a circuit structure comprising a semiconductor layer 1, a source region and a drain region 6, 7 and a channel region located between the source/drain regions;

a gate oxide layer located on a surface of the channel region, the entire said gate oxide layer having a substantially uniform thickness; and

a gate electrode located on a portion of said gate oxide layer 22 above said channel region, said gate oxide layer extends outwardly from both sides of said gate electrode, wherein the portion of said gate oxide layer located only beneath said gate electrode has first and second portions, said first portion is adjacent said drain region, said second portion (part of layer 12) comprises all remaining portions of said gate oxide layer located under said gate electrode and has first and second sides, said first side is adjacent said first portion and said second side is adjacent said source region,

and said first portion has a higher ion implant concentration (of hydrogen) higher than in said second portion and all remaining portions of said gate oxide layer extending outwardly from both sides of said gate electrode.

Claim Rejections - 35 USC § 102/103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1, 3, and 5-7 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kusunoki et al.

Kusunoki et al. teach in figure 11 and related text a circuit structure comprising a semiconductor layer 1; a source region and a drain region 6, 7 in the semiconductor

layer which are lightly doped and heavily doped with a first conductivity-type dopant; a channel region located between the source/drain regions;

an oxide layer formed on the semiconductor layer, the entire said oxide layer having a substantially uniform thickness;

a gate electrode formed on a portion of the oxide layer and having first and second leading edges, said gate oxide layer extends outwardly from both sides of said gate electrode, and

where a portion of the oxide layer defines a first overlap region 22 which is beneath the gate electrode and adjacent the first leading edge and inward of the second leading edge and a second overlap region 12 comprising all remaining portions of the oxide layer located beneath said gate structure, said second overlap region having first and second sides, said first side being adjacent said first overlap region and said second side being adjacent said second leading edge and adjacent the drain region, the overlap region having an ion implant concentration (of hydrogen) higher than in said second overlap region 12 and all remaining oxide layer portions extending outwardly from both the first and second leading edges of the gate structure, and which can be effective to lower the surface electrical field in the overlap region.

Kusunoki et al. do not explicitly state that the impurity concentration is sufficient to lower the surface electrical field in the overlap region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use sufficient impurity concentration in Kusunoki et al.'s device to lower the surface electrical field in the overlap region in order to improve the device characteristics.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 8-9, 47, 49-53 and 55-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al. in view of Akram.

Regarding claims 8-9 and 52-53, Kusunoki et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a gate stack. Akram teaches a gate electrode being a gate stack 104 comprising polysilicon and one or more additional layers 22 selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks) having first and second leading edges located on a portion of the gate oxide layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate electrode comprising a gate stack electrode 104 comprising polysilicon and one or more additional layers 22 selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks) having first and second leading edges located on a portion of the gate oxide layer, in Kusunoki et al.'s device, in order to reduce the contact resistance of the device.

Regarding claims 47 and 55, Akram et al. teach a channel region between a pair of filed isolation regions, wherein all remaining gate oxide layer portions extending between said pair of filed isolation regions.

Regarding claim 56, Kusunoki et al. teach in figure 44 source and drain regions each having first and second dopants wherein the second dopant extending deeper into the semiconductor layer than the first dopant.

Claims 10 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al. in view of Admitted Prior Art (APA).

Kusunoki et al. teach substantially the entire claimed structure, as applied to claims 3 and 47 above, except a gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer. APA teaches in figure 1 a gate electrode is comprised of a layer of polysilicon 18, a layer of titanium nitride 20 deposited on the polysilicon layer, and a layer of tungsten 22 deposited on the titanium layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate electrode comprising of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer in Kusunoki et al.'s device, in order to reduce the contact resistance of the device.

Claims 11-12,14 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al. in view of Motoyoshi et al. (JP 6-53492).

Regarding claim 12, Kusunoki et al. teach substantially the entire claimed structure, as applied to claim 3 above, except using the transistor in a CMOS configuration. Motoyoshi et al. use a transistor having a gate oxide comprising fluorine in a CMOS configuration. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Kusunoki et al.'s transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

Regarding claims 11 and 57, Motoyoshi et al. teach in figure 7 a pair of conductive studs and an interlevel dielectric layer provided on the semiconductive layer, the interlevel dielectric layer have a pair of through holes, each accommodating one of each the pair of conductive studs, and one of each the pair of conductive studs contacting one of each the source/drain regions. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a pair of conductive studs through an interlevel dielectric layer provided on the semiconductive layer, the interlevel dielectric layer have a pair of through holes, each accommodating one of each the pair of conductive studs, and one of each the pair of conductive studs contacting one of each the source/drain regions in Kusunoki et al.'s device in order to operate the device in its intended use. Note that the device would not operate without external connections.

Allowable Subject Matter

Claims 2, 4, 13, 46 and 48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-14 and 45-57 have been considered but are moot in view of the new ground(s) of rejection and the allowance of claims 2, 4, 13, 46 and 48.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
10/12/06

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PRIMARY EXAMINER
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